UNITED STATES PATENT AND TRADEMARK OFFICE

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EXAMINER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2008*.
2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 21-30* is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-19, 21-30* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All   b)☐ Some * c)☐ None of:
        1.☐ Certified copies of the priority documents have been received.
        2.☐ Certified copies of the priority documents have been received in Application No. _____.
        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This application has been examined. Claims 1-19,21-30 are pending. Claim 20 is cancelled.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/02/2008 has been entered.

Priority

The effective date of the claims described in this application is March 29, 2004.

Information Disclosure Statement

The Applicant is respectfully reminded that each individual associated with the

filing and prosecution of a patent application has a duty of candor and good faith in

dealing with the Office, which includes a duty to disclose to the Office all information

known to that individual to be material to patentability as defined in 37 CFR 1.56.

There were no information disclosure statements filed with this application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11, 14-18, 28-30 rejected under 35 U.S.C. 103(a) as being

unpatentable over Narasimhan (US Patent 6446192) in view of Bishop (US Patent

4914653), or alternatively, Bishop in view of Narasimhan.

Narasimhan disclosed (re. Claim 1) a management port for a wireless device

platform, comprising: a communication link (Narasimhan-Figure 7 , Column 6 Lines 30-

35, *'network interface chip'*) for the wireless device platform, (Narasimhan-Column 3

Lines 15-20) the communication link to provide an inbound link and an outbound link,

(Narasimhan-Column 13 Lines 40-50) and to control data flow over the inbound and

outbound links; and

a management block to receive command data *from the at least one processor*

or peripheral through a predetermined logic channel in the inbound link, the

management (Narasimhan-Figure 7, '*command processor*') through a channel in the

inbound link and generate a corresponding command signal on a microprocessor bus

system (Narasimhan-Figure 9,Column 13 Lines 55-65, Column 14 Lines 30-35) that is

local to the command link to perform a management function for the microprocessor

system, (Narasimhan- Column 14 Lines 30-35,'*microcontroller*') the management block

being further adapted to receive a response signal from the bus and transmit

corresponding response data through a channel in the outbound link. (Narasimhan-

Column 13 Lines 40-50)

Narasimhan disclosed (re. Claim 1) a communication link, local to a

microprocessor subsystem. (Narasimhan-Figure 2,Column 14 Lines 30-35,'*the internal*

data bus of the NIC connects directly to the device data bus').

Narasimhan disclosed (re. Claim 1) the microprocessor subsystem comprising

a processor core and at least one processor subsystem, and a microprocessor bus

system, (Narasimhan-Figure 9,Column 13 Lines 55-65, Column 14 Lines 30-35) the

microprocessor bus system providing a communication path between the processor

core and the at least one processor subsystem; (Narasimhan-Figure 9)

Narasimhan disclosed (re. Claim 1) *the inbound link providing a path for*

communications from the inter- processor bus to a peripheral bus (Narasimhan-Column

14 Lines 25-35) *of the microprocessor subsystem, the inbound link receiving*

communications from at least one processor or peripheral communicating over the inter-

processor bus, (Narasimhan-Column 13 Lines 40-50)

the outbound link providing a path for communications from the peripheral bus of

the microprocessor subsystem to the inter-processor bus, (Narasimhan-Column 14

Lines 25-35) *the outbound link transmitting communications over the inter-processor*

bus to the at least one processor or peripheral, (Narasimhan-Column 13 Lines 40-50)

While Narasimhan substantially disclosed the claimed invention Narasimhan did

not disclose (re. Claim 1) inter-processor communication and using logic channels.

Bishop disclosed (re. Claim 1) inter-processor communication and using logic

channels. (Bishop-Column 6 Lines 55-65)

Narasimhan and Bishop are analogous art because they present concepts and

practices regarding interfaces for multi-processor systems. At the time of the invention

it would have been obvious in the networking art to combine Bishop into Narasimhan.

The motivation for said combination would have been to minimize latency (Bishop-

Column 2 Lines 15-20).

Claims 8,15,28 are rejected on the same basis as Claim 1.

Narasimhan-Bishop disclosed (re. Claim 28) the multi-channel (Bishop-Column

6 Lines 55-65) inbound link providing a path for communications from the inter-

processor bus to a peripheral bus of the microprocessor system, (Narasimhan-Column

13 Lines 40-50) the multi-channel inbound link receiving communications from at least

one processor or peripheral communicating over the inter-processor bus, (Narasimhan-

Column 14 Lines 25-35)

the multi-channel (Bishop-Column 6 Lines 55-65) outbound link providing a path

for communications from the peripheral bus of the microprocessor system to the inter-

processor bus, (Narasimhan-Column 13 Lines 40-50) the multi- channel outbound link

transmitting communications over the inter-processor bus to the at least one processor

or peripheral; (Narasimhan-Column 14 Lines 25-35)

Narasimhan-Bishop disclosed (re. Claim 2,17,29) wherein the communication

link includes a physical layer to provide both the inbound and outbound links

(Narasimhan-Column 13 Lines 40-50) with multiple logic channels, (Bishop-Column 6

Lines 55-65) and a data link protocol to control data flow over the inbound and output

links, (Narasimhan-Column 13 Lines 40-50) and

*the management block provides the corresponding command signal directly on
the microprocessor bus.* (Narasimhan-Column 14 Lines 25-35)

Narasimhan-Bishop disclosed (re. Claim 3,9) wherein the management function

includes a debug function. (Narasimhan-Column 1 Lines 20-25,Column 14 Lines 60-

65,'*STATUS registers provide information about errors*')

Narasimhan-Bishop disclosed (re. Claim 4,10) wherein the management function

includes accessing memory. (Narasimhan-Column 17 Lines 45-55, '*the variable is

identified and the device processor writes the value to the network interface chip*')

Narasimhan-Bishop disclosed (re. Claim 5,11) wherein the management function

includes accessing configuration registers. (Narasimhan-Column 16 Lines 55-65)

Narasimhan-Bishop disclosed (re. Claim 6) wherein the management function

includes accessing a peripheral device of the microprocessor system. (Narasimhan-

Column 14 Lines 20-25,'other device peripherals')

Narasimhan-Bishop disclosed (re. Claim 7,16,30) wherein the management block

includes: a command register connected to the bus and to the communication link,

(Narasimhan-Column 14 Lines 60-65,'commands are written to the WRITE DATA

register') the command register to temporarily store the command data delivered

through the predetermined logic channel in the inbound link; a response register

connected to the bus and to the communication link, the response register to

temporarily store response data from the bus; (Narasimhan-Column 14 Lines 60-

65,'received data are read from the READ data register') and a manageability controller

connected to the microprocessor bus, the command register, and the response register,

the manageability controller (Narasimhan-Column 6 Lines 30-40) being adapted to

determine when command data is received at the command register and to transmit the

corresponding command signal over the bus, and further being adapted to receive the

response signal from the bus and store corresponding response data at the response

register, and to transmit the response data through the predetermined logic channel in

the outbound link.(Narasimhan-Figure 7,Column 13 Lines 40-50)

Narasimhan-Bishop disclosed (re. Claim 14)   the management block being

adapted to generate the corresponding command signal on the at least one bus to

perform a management function for the at least one peripheral device. (Narasimhan-

Column 6 Lines 30-40)

Narasimhan-Bishop disclosed (re. Claim 18) wherein the embedded

communications microprocessor system is adapted to wirelessly communicate with at

least one other devices. (Narasimhan-Column 3 Lines 15-20)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12,13, 19,21-27 rejected under 35 U.S.C. 103(a) as being unpatentable

over Narasimhan (US Patent 6446192) in view of Bishop (US Patent 4914653) further

in view of Balachandran (US Publication 20050078620).

Narasimhan-Bishop disclosed   (re. Claim 19) an inter-processor communication

bus connected to the communication links of both the applications microprocessor

system and the communications microprocessor system, as disclosed in the rejection

for Claim 1.

Furthermore Narasimhan-Bishop disclosed (re. Claim 19) *the inbound link*

providing a path for communications from the inter- processor bus to a peripheral bus

(Narasimhan-Column 14 Lines 25-35) *of the microprocessor subsystem, the inbound*

link receiving communications from at least one processor or peripheral communicating

over the inter- processor bus, (Narasimhan-Column 13 Lines 40-50)

the outbound link providing a path for communications from the peripheral bus of

the microprocessor subsystem to the inter-processor bus, (Narasimhan-Column 14

Lines 25-35) *the outbound link transmitting communications over the inter-processor*

bus to the at least one processor or peripheral, (Narasimhan-Column 13 Lines 40-50)

Furthermore Narasimhan-Bishop disclosed (re. Claim 19) a *manageability port:*

being adapted to receive command data from the at least one processor or peripheral

through a predetermined logic channel in the inbound link,

providing a corresponding command signal on the microprocessor bus, and further is

adapted to receive a response signal from the microprocessor bus, and

transmitting corresponding response data through a predetermined logic channel in the

outbound link to the at least one processor or peripheral via the inter-processor bus.

(see rejection for Claim 1)

While Narasimhan-Bishop substantially disclosed the claimed invention

Narasimhan-Bishop did not disclose   (re. Claim 19) a substantially omni-directional

antenna connected to the embedded communications microprocessor system; (re.

Claim 12) wherein the at least one processor subsystem includes a security module;

(re. Claim 13) wherein the at least one processor subsystem includes a Universal Serial

Bus (USB) client

Balachandran disclosed (re. Claim 19) a substantially omni-directional antenna

connected to the embedded communications microprocessor system. (Balachandran-

Paragraph 8 Figure 1)

Balachandran disclosed (re. Claim 12) wherein the at least one processor

subsystem includes a security module (Balachandran-Paragraph 50)

Balachandran disclosed (re. Claim 13) wherein the at least one processor

subsystem includes a Universal Serial Bus (USB) client. (Balachandran-Paragraph 33,

Figure 4)

Narasimhan,Bishop and Balachandran are analogous art because they present concepts and practices regarding interfaces for multi-processor systems. At the time of the invention it would have been obvious in the networking art to combine Balachandran into Narasimhan-Bishop. The motivation for said combination would have been to enable separation of the access functionality and the application functionality as implemented in two separate processors. (Balachandran-Paragraph 32)

Narasimhan-Bishop-Balachandran disclosed (re. Claim 21) wherein the embedded communications microprocessor system includes a microprocessor system adapted to wirelessly communicate with at least one other device. (Narasimhan-Column 3 Lines 15-20)

Narasimhan-Bishop-Balachandran disclosed (re. Claim 22) wherein the microprocessor system is adapted to wirelessly communicate with at least one other devices using IEEE 802.11 technology. (Balachandran-Paragraph 33, Figure 4)

Narasimhan-Bishop-Balachandran disclosed (re. Claim 23) wherein the microprocessor system is adapted to wirelessly communicate with at least one other device using cellular radio technology. (Balachandran-Paragraph 33, Figure 4)

Narasimhan-Bishop-Balachandran disclosed (re. Claim 24) wherein the microprocessor is adapted to wirelessly communicate using general packet radio service (GPRS) technology. (Balachandran-Paragraph 33, Figure 4)

Narasimhan-Bishop-Balachandran disclosed (re. Claim 25) wherein the microprocessor is adapted to wirelessly communicate using code division multiple access (CDMA) technology. (Balachandran-Paragraph 35, 'standard wireless technologies')

Narasimhan-Bishop-Balachandran disclosed (re. Claim 26) wherein the microprocessor is adapted to wirelessly communicate using wideband code division multiple access (WCDMA) technology. (Balachandran-Paragraph 35, 'standard wireless technologies')

Narasimhan-Bishop-Balachandran disclosed (re. Claim 27) a microprocessor system adapted to wirelessly communicate with at least one other devices using an IEEE 802.11 technology; and a microprocessor system adapted to wirelessly communicate with at least one other device using cellular radio technology. (Balachandran-Paragraph 33, Figure 4)

Response to Arguments

Applicant's arguments filed 07/24/2008 have been fully considered but they are

not persuasive.

The Applicant presents the following argument(s) [in italics]:

[In Narasimhan] the NIC appears to the processor as simply another slave

peripheral device.

The Examiner respectfully disagrees with the Applicant. Narasimhan Column 17

Lines 40-65 disclosed an embodiment wherein the NIC functions as a control relay in

order to control the peripheral devices and thus is not a slave peripheral device.

The Applicant presents the following argument(s) [in italics]:

... the processor communicates to the NIC over a system bus through the

processor's communication port using the appropriate protocol for the system inter-

processor bus and does not communicate directly over the micropocessor bus system

that provides a communication path between the processor core and at least one

processor subsystem

The Examiner respectfully disagrees with the Applicant. Narasimhan Figure

2,Column 14 Lines 30-35 disclosed wherein *'the internal data bus of the NIC connects*

directly to the device data bus'.   Where the NIC is able to control the peripheral

devices in monitoring and control mode (Narasimhan Column 17 Lines 40-65) and

provide several local device interfaces (Column 16 Lines 5-25) the Examiner thus

concludes that Narasimhan *communicates directly over the micropocessor bus system*

that provides a communication path between the processor core and at least one

processor subsystem.

The Applicant presents the following argument(s) [in italics]:

...management block could receive, through a predetermined channel, command

data. Subsequently, the management block could issue a command to the processor

core over microprocessor bus, thus by-passing the peripheral bus. Narasimhan fails to

disclose or render obvious a management block or similar device that is capable of

producing such command...

The Examiner respectfully disagrees with the Applicant.

In response to applicant's argument that the references fail to show certain

features of applicant's invention, it is noted that the features upon which applicant relies

(i.e., *by-passing the peripheral bus*) are not recited in the rejected claim(s). Although

the claims are interpreted in light of the specification, limitations from the specification

are not read into the claims.

Furthermore Narasimhan Column 17 Lines 20-65 disclosed *a management*

block or similar device that is capable of producing such command that is issued to the

processor core over microprocessor bus, thus by-passing the peripheral bus.

Conclusion

Examiner's Note: Examiner has cited particular columns and line numbers in

the references applied to the claims above for the convenience of the applicant.

Although the specified citations are representative of the teachings of the art and are

applied to specific limitations within the individual claim, other passages and figures

may apply as well. It is respectfully requested from the applicant in preparing

responses, to fully consider the references in entirety as potentially teaching all or part

of the claimed invention, as well as the context of the passage as taught by the prior art

or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully

requested to indicate the portion(s) of the specification which dictate(s) the structure

relied on for proper interpretation and also to verify and ascertain the metes and bounds

of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Greg Bengzon whose telephone number is (571) 272-3944. The examiner can normally be reached on Mon. thru Fri. 8 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Vaughn can be reached on (571)272-3922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Greg   Bengzon/

Examiner, Art Unit 2444